WHAT IS CLAIMED IS:

1. An apparatus, comprising:

a current directing circuit comprising:

a first write head connection node; and

a second write head connection node;

wherein the current directing circuit is adapted to provide current to the first write head connection node and to the second write head connection node; and

a common mode generator, coupled to the current directing circuit, adapted to provide additional current to the first write head connection node and to the second write head connection node;

wherein the first write head connection node is adapted to produce a first write signal;

wherein the second write head connection node is adapted to produce a second write signal;

wherein the current and the additional current are adapted to establish a voltage across the first write head connection node and the second write head connection node;

wherein the voltage is adapted to be pulled toward a first polarity based on the first write signal and toward a second polarity based on the second write signal; and

wherein the voltage pulled toward the first polarity and the voltage pulled toward the second polarity are substantially centered about a common mode voltage.

2. The apparatus of claim 1, wherein the current and the additional current are provided contemporaneously.

3. The apparatus of claim 1, wherein the current and the additional current are provided independently.

4. The apparatus of claim 1, wherein the voltage across the first write head connection node is pulled toward a positive supply voltage.

5. The apparatus of claim 1, wherein the voltage across the second write head connection node is pulled toward a negative potential.

6. The apparatus of claim 1, wherein the voltage is adapted to be pulled toward the first polarity for a first duration, and wherein the voltage is adapted to be pulled toward the second polarity for a second duration.

7. The apparatus of claim 6, wherein the first duration and the second duration are unequal.

8. The apparatus of claim 6, wherein the first duration and the second duration are substantially equal.

9. The apparatus of claim 6, wherein the first duration and the second duration overlap.

10. A preamplifier, comprising:

a common mode generator;

an H-bridge circuit;

a current mirror coupled to the common mode generator and to the H-bridge circuit;

an overshoot system coupled to the current mirror and the H-bridge circuit;

a first write head connection node adapted to produce a first write signal, wherein the first write head connection node is coupled to the H-bridge circuit; and

a second write head connection node adapted to produce a second write signal, wherein the second write head connection node is coupled to the H-bridge circuit;

wherein the common mode generator is adapted to provide current;

wherein the current is adapted to establish a voltage across the first write head connection node and the second write head connection node;

wherein the voltage is adapted to be pulled toward a first polarity based on the first write signal and toward a second polarity based on the second write signal; and

wherein the voltage pulled toward the first polarity and the voltage pulled toward the second polarity are substantially centered about a common mode voltage.

11. The preamplifier of claim 10 further comprising a first current source coupled to the common mode generator.

12. The preamplifier of claim 11, wherein the first current source supplies current to the current mirror when the first current source is at a maximum level.

13. The preamplifier of claim 11, wherein the first current source supplies current to the common mode generator when the first current source is not at a maximum level.

14. The preamplifier of claim 13, wherein the current is supplied substantially equally to the first write head connection node and to the second write head connection node.

15. The preamplifier of claim 14, wherein the common mode voltage remains substantially constant when the current is supplied substantially equally to the first write head connection node and to the second write head connection node.

16. The preamplifier of claim 11, wherein the first current source is a digital to analog converter.

17. The preamplifier of claim 11, wherein the first current source comprises at least one current source.

18. The preamplifier of claim 11, wherein the first current source is programmable.

19. The preamplifier of claim 11 further comprising a second current source coupled to the overshoot system.

20. The preamplifier of claim 19, wherein the overshoot system supplies current to the first write head connection node and to the second write head connection node.

21. The preamplifier of claim 19, wherein at least a portion of the common mode generator is off for a period of time when at least a portion of the overshoot system is on.

22. The preamplifier of claim 21, wherein one of the following voltages from a group comprising of: the voltage pulled toward the first polarity, and the voltage pulled toward the second polarity is pulled in one of a following direction from a group comprising of: higher, and lower, from the substantially centered common mode voltage.

23. The preamplifier of claim 11, wherein the first write signal and the second write signal are received by a write head external to the preamplifier via an interconnect coupled between the preamplifier and the write head.

24. An apparatus, comprising:

a current directing circuit comprising and adapted to provide current to :

a first write head connection node; and

a second write head connection node; and

a common mode generator, coupled to the current directing circuit, adapted to provide additional current to the first write head connection node and to the second write head connection node;

wherein the current and the additional current are adapted to establish a voltage across the first write head connection node and a voltage across the second write head connection node; and

wherein the voltage pulled toward the first polarity and the voltage pulled toward the second polarity are substantially centered about a common mode voltage.

25. A method for producing write signals, comprising:

receiving current from a current source at a first system when the current source is not operating at a maximum current output;

supplying the current from the first system to a second system;

decreasing a voltage level at a transistor in the second system based on the supplied current;

decreasing a voltage level at a write connection node coupled to the transistor based on a decreased current; and

maintaining a substantially common voltage for positive excursions and negative excursions of a write signal at the write connection node based on the decreased voltage level at the write connection node.

26. The method of claim 25 further comprising receiving current from the current source at the second system when the current source is not operating at the maximum current output.

27. The method of claim 25 further comprising receiving current from the current source at the second system when the current source is operating at a maximum current output.

28. The method of claim 26 further comprising contemporaneously receiving the current at the first system and at the second system.

29. The method of claim 26 further comprising receiving the current from the current source at the transistor.

30. The method of claim 25 further comprising decreasing a bias point of the transistor.

31. The method of claim 30 further comprising decreasing the voltage level at the write connection node coupled to the transistor based on the decreased bias point.

32. A method for producing write signals, comprising:

receiving current from a current source at a first system when the current source is not operating at a maximum current output;

supplying the current from the first system to a second system;

maintaining a voltage level at a transistor in the second system based on the supplied current;

maintaining a voltage level at a write connection node coupled to the transistor based on a decreased bias point of the transistor; and

maintaining a substantially common voltage for positive excursions and negative excursions of a write signal at the write connection node based on the decreased voltage level at the write connection node.